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Research and Design of Portable Fault Recorder Based on FPGA

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Abstract

Facing the lack of traditional fault recorder technology and according to data collection requirements of the fault analysis of power system, this article established a new type of portable recorder that was designed surrounding FPGA. The fault recorder abandoned the "multi-layer structure" and used single FPGA chip and embedded CPU core to complete the master function. This designed fault recorder can run independently from the computer and had the features of small size, light weight, higher degree of integration and so on. □

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1. Introduction

With the growing demand for electricity, the power system is developing toward complexity, expansion and intelligent. So the analysis on the fault of the power system also seems increasingly important. In the process of development of power system, fault recording technology as essential to fault analysis of power system made considerable progress. But traditional fault recorder had many problems such as less sampling rate and lower accuracy and so on, and it had not qualified for the needs of the fault recorder of the current power system. Small and medium power monitoring equipment and industrial site power monitoring made a number of requirements on fault recorder, such as high sampling rate and high sampling precision, and being able to save more information about the fault and before and after the fault. Meanwhile it also made portable requirement on the fault recorder[1,2,3]. According to data collection requirements of the fault analysis of power system, this article established a new type of portable fault recorder that was designed surrounding FPGA. FPGA is the core of the system. Through circuit expansion on the data acquisition circuit, human-computer interaction (HCI) and communication circuit,

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the system achieves high-speed and high-precision acquisition and transmission of fault data. The fault recording device known as a "black box" of power system is essential safe automatic device for power monitoring, and it has a very important significance for security and stability of the power system.

2. Systems Architecture

The hardware of the portable recorder consists of five parts that are sensor circuit board, data acquisition circuit board, FPGA system board, LCD display and keyboard, communication device and power adapter. The structure is shown in Fig. 1.

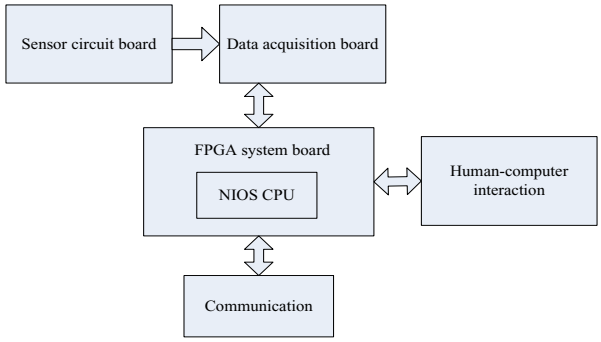

Fig. 1. The composition of embedded fault recorder

This design uses embedded technology and put the High-speed, high-capacity FPGA devices as the core design. Through using high-speed, high-precision analog components, it try to achieve high-quality acquisition of fault signal of power system[4].By using digital signal processor (DSP) Builder, SOPC Builder and other design tools, the design completes system-on-programmable chip (SOPC, System On Programmable Chip), digital filtering, fast Fourier transform (FFT, Fast Fourier Transform) and other modules.

3. The Hardware Design of Fault Recording Device

In the process of Hardware design, the paper adopts the idea of modular design, hoping the device interference, electromagnetic compatibility, insulation performance in line with national standards. The specific design parameters are:

(1) 16-bit precision is 16 simultaneous analog acquisition channels (0.5), single-channel maximum sampling frequency is 200Ksps, full channel maximum sampling frequency is 20Ksps;

(2) 16-way switch channels, which open into the 8, 8 out of capacity;

(3) The objects of the collection for analog acquisition channels are each phase current and voltage amplitude, phase, etc., the objects of the collection for switch acquisition channels are protection of relay and the act of switching, etc;

(4) The starting modes of device are manual and automatic modes, including automatic start mode for the mixed analog and digital triggering, to improve its reliability;

(5) The device has strong network functions and communications capabilities, and by using USB and other means of communication, it can achieve high-speed transmission of fault data;

(6) Using the custom CPU technology of single FPGA chip and to the core of embedded system design to achieve measurement of high sampling rate and accuracy of data.

Design uses field programmable gate array (FPGA, Field-Programmable Gate Array) as the main processor, which external expansion circuit is responsible for ensuring the normal operation of FPGA and these things consisted of the logic resources in its on-chip such as data acquisition controller, digital signal processing modules, HCI and communication module[5,6].

The Voltage, current transformer in data acquisition circuit mainly plays the role of buck and isolation, which connects the acquisition circuit and the collected signal, and it is the main isolation device between fault recording instrument and the power system, ensuring the safe operation of equipment and safe operation of the operators; After the voltage, current transformer reduced the amplitude of the analog signal into less than 10V, then through adjusting circuit which can adjusted Voltage amplitude of the analog signal into the acceptable range of Analog to Digital Converter (ADC), the analog filter circuit channel filter out unwanted high frequency interference signals; ADC digitized the analog signal and put the digital signal send to FPGA to process and store it correspondingly.

HCI Module provides a good operating environment for operators, to improve the controllability of the device and monitor each electrical parameters of power system on maximum. This design uses the keyboard and LCD as interactive tools of HCI. Traditional fault recorder used a single serial communication, its data transmission rate is lower, and do not have the network communication function. To compensate for this deficiency, we use both USB and Ethernet communication, which effectively solve real-time transmission problem of the data collected by fault recorder.

4. The Software Design of System

The Software Design of System design includes mainly software design of μC / OS-II operating system, logic design of user and the design of digital signal processing programming in three parts. The software design of μC/ OS-II operating system belongs to the one of system application program, and the designs of the user logic code and digital signal processing program is the underlying driver design. Application program based on μC / OS-II operating system is realized by using the C language, the underlying driver is realized by using a hardware description language (Verilog HDL). Software design level of overall system is constituted by operational system layer, system task layer, bottom drive layer and hardware platform. System task layer includes SD card reader, data processing, communication and start-up criterion, etc. Bottom drive layer includes ADC IP core, PS/II IP core, VGA IP core, digital signal processing module and so on (see Fig. 2).

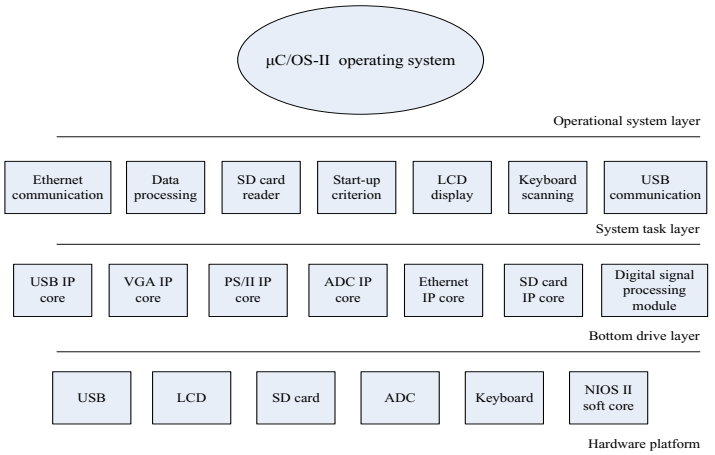

Fig. 2. Software design hierarchical graph of overall system

4.1. μC / OS-II operating system

Embedded key-machine is realized on the basis of μC / OS-II embedded operating system, which is a preemptive priority-based embedded real time operating system (RTOS) and can run on 8-64 on a variety of CPU. μC / OS-II can manage 64 tasks, among which, except eight tasks as a system to retain the tasks, the remaining 56 tasks can be dominated by the user, and the μC / OS-II provides mailboxes, message queues, semaphores, and other system services[7].

In the design, the system is divided into six tasks, that is, SD card reader, data acquisition, keyboard scanning, USB and Ethernet communications, and LCD display. In the state of recording, SD card reading and writing control tasks is responsible for the original data and processed by the digital signal data storage; when it works in communicating with the host computer, it is responsible for the preservation of data output. The role of Data acquisition and control tasks is to turn the acquisition parameters into a control signal after the user re-sets the sampling parameters, and to notify the data acquisition module to change the acquisition parameters. USB and Ethernet communication module is mainly responsible for communication with the host computer, and USB can also store data. LCD display task is mainly responsible for real time display collected by the original signal; keyboard scanning task completes the task of detecting the keyboard, to achieve HCI, and to ensure the smooth completion of user action.

4.2. The design of user logic code

In the system, NIOS II is as Main Processor, μC / OS-II runs on top of NIOS II. Between soft core NIOS II and Peripherals of the system there is Avalon which links NIOSII with peripheral control IP, and based on peripheral timing requirements and control methods, the user writes the control IP of Avalon timing. NIOS II complete control of IP peripherals of system through operating IP[8].The method's portability is very strong, and through automatic configuration of SOPC Builder, you can use the minimum FPGA resources to obtain the best change structure of Avalon.

All of peripherals connected with FPGA required making relevant logic code design in accordance with their timing characteristics. Some parts of the design among them have been integrated under development environment of Quartus II. In the design we only require making relevant logic code design to ADC, analog switches and some other peripherals.

4.3. The design of digital signal processing

Digital signal processing measures and analyzes analog signal among of which are mainly discrete Fourier transform, fast Fourier transform and digital filtering. In these treatment methods a large number of multiplication are needed. Therefore, in order to improve the efficiency of digital signal processing, the processor multipliers need to be considered when selecting the appropriate processor, meanwhile pipeline structure also help improve the speed of digital signal processing. On the premise that the processing speed, digital signal processing often requires the use of computer or dedicated processing devices such as a DSP, application specific integrated circuit (ASIC) and so on.

However, DSP device is the cost of higher prices, compared with the general purpose microprocessor components, its generic function is relatively weak. And it is hard to communicate with other devices; this brings some difficulties for the design. So in the design, through using some of FPGA logic resources to form digital signal processing module, we complete digital signal processing functions, and in the premise of ensuring the processing speed, we reduced hardware costs and shorten the design cycle, reduce the design difficulty.

4.4. *Data processing and design of starting criterion*

The purpose of signal processing, usually two: one is the analysis of signal characteristics, that is, to obtain the signal characteristics parameters; the other is the signal conversion, that is, to transform the original form of the signal into the one that can meet some particular requirement. This design mainly uses fast Fourier transform, to analyze the frequency characteristics and characteristics parameters of the signal or system.

In the real system, the data collected by ADC are real numbers. In order to improve efficiency, people often put together two N point real sequences to form an N point FFT to compute. Its basic principle is to use the even and odd symmetry of discrete Fourier transform of the complex sequence[9,10,11].During the FFT computation the main problem is reverse order and butterfly algorithm. Reverse order is based on the principle of Code bit inversion to achieve, which is a prerequisite for the Butterfly algorithm, while the Butterfly algorithm is the key of FFT. There in the function library can call the FFT library functions, library functions can be used to complete the FFT computation.

Fault recording device has the functions to ascertain the system failures to start recording automatically and stop recording when troubleshooting, but also by external command to start and stop. The starting criterion is the core of data computing of Recorder device. The various starting methods of the design are summarized: (1) the amount of mutation is beyond the limits; (2) effective numerical is beyond the limits; (3) symmetry is beyond the limits; (4) frequency and frequency rate; (5) the amount of switch starts; (6) local manually start and remote command start; (7) fault recording lasts longer than 3S, or all of the startup volume reduction, then the operation of recording stops.

7 of above are the basis of starting and stopping of fault recording, the mutation quantity, effective numerical, symmetrical components and the frequency are the four key indicators to determine fault.

5. Systems Test

In order to develop more friendly display interface, the system uses UCGUI aided design. UCGUI is the universal interface software for embedded graphics, which provides independent interface program outside the processor and LCD controller. Its source code is freely available to the users [12].

Firstly we set the standard effective voltage to 220V, and input 225V effective voltage signal. The system runs normally for some time. We raise the effective voltage value to 250V artificially. The device can automatically start recording waves. And the log interface shows the voltage beyond the boundaries and prompts failure. Secondly the device runs normally for some time, and we artificially lower a way switch. The device can also automatically start recording waves. The log interface shows the appropriate switch and prompts failure.

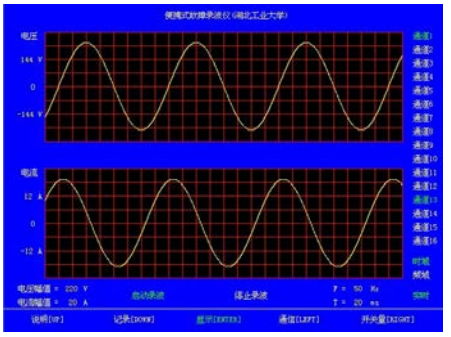

Fig. 3. Waveform display of recorded data

In Fig.3, it is a real-time time-domain recorded waveform during operation of the device. Both channels record waveforms at the same time, taking the channel 1 voltage signal measured peak to 220V and taking the channel 13 current signal measured peak to 20A. Voltage and current signals are both the standard trouble-free band sine waves, and can be stored directly. By computing analysis, the effective voltage value is 155.56V and the effective current value is 14.14A. The frequency of two signals is 50 Hz and two time interval is 20ms. The system works well in the test phase, and achieves to the relevant national technical standards basically.

6. Conclusion

After nearly two years of design, development, test, and debug, the project has been almost completed. This Portable instrument designed for fault recording, is different from the existing design architecture, and in the following areas it has its own characteristics:

(1) Faster sampling rate, higher sampling precision, and the advantages of portability. It can keep record of the more abundant information for analysis of power failure;

(2) Using "embedded" approach, the recording devices designed is completely free from computer system and windows system, and able to operate independently. And let the size and weight reduce to achieve" portable" goals;

(3) Hierarchical structure aside, using a single-chip FPGA, it achieves further high-density functional integration of fault recording equipment.

FPGA has been applied in the present fault recorder, but mainly deals with the logic coordination between multi-chips; this does not play a main advantage of FPGA – "the area for speed, area for performance."

In theory, as long as with enough "space", FPGA can achieve a variety of customized, integrated functions; FPGA can be embedded 32-bit CPU core; its performance is no less than the ARM chip, and its application is more convenient, single-core or multi-core can be designed freely. An FPGA chip is possible to achieve all the required fault recorder function, which will save the data transmission links in the stratified layer, reduce hardware costs, improve real-time.

7. Acknowledgments

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